Princeton Technology Corp.
Tel: 886-2-29162151
Fax 886-2-29174598
URL: *http://www.princeton.com.tw*

Description

PT2313L is a four-channel digital control audio processor utilizing CMOS Technology. Volume, Bass, Balance, Front/Rear Fader Processor, Selectable Input Gain are incorporated into a single chip having the highest performance and reliability with the least external components. All functions are programmable using the I^2C Bus. PT2313L is housed in 20-pin or 28-pin DIP/SOP Package. The 28-pin version provides additional Two Band Tone Control and Loudness Function and is pin-to-pin compatible with TDA7313. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

Features

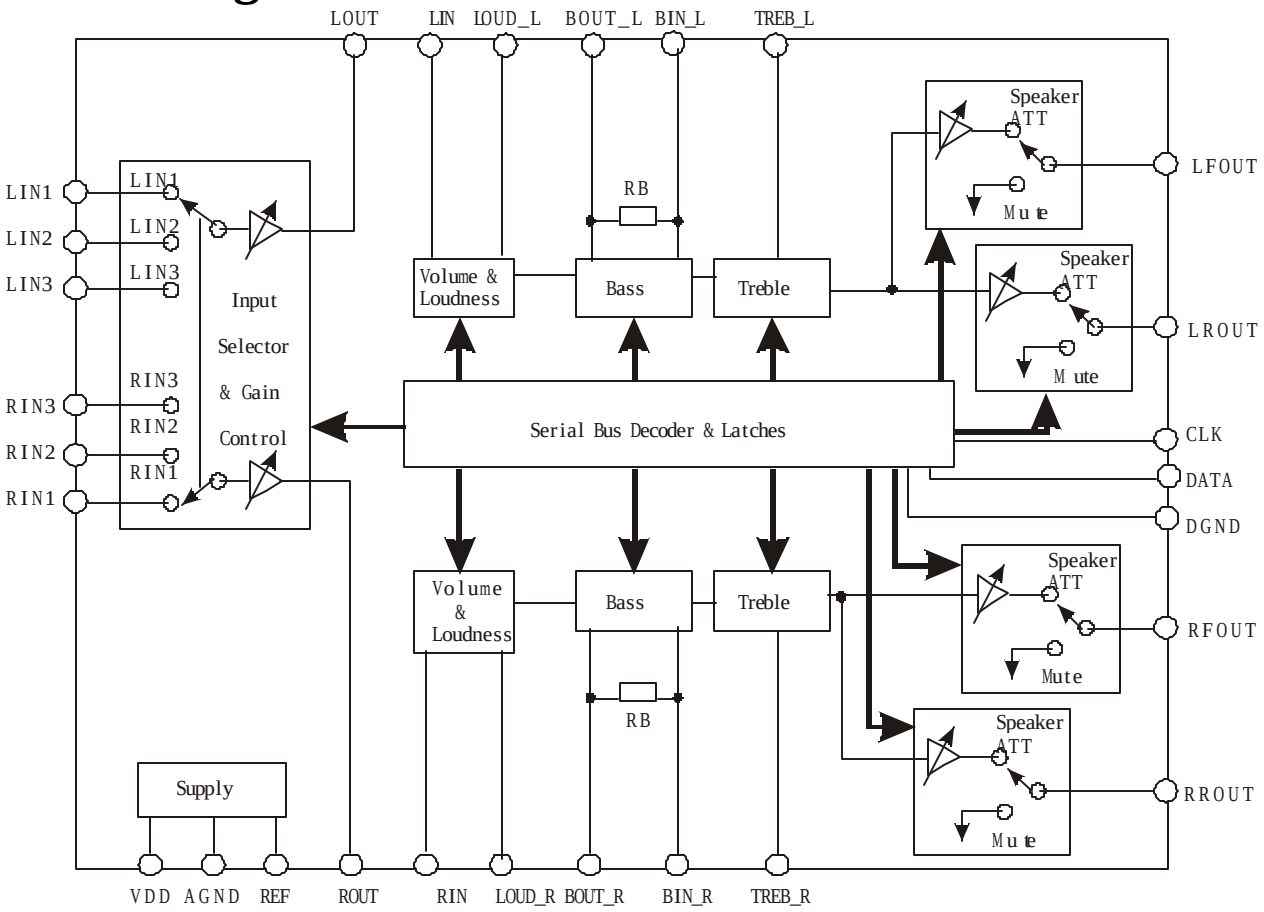
- CMOS Technology
- Least External Components
- Treble and Bass Control (available only in the 28-pin version)
- Loudness Function (available only in the 28-pin version)
- 3 Stereo Inputs with Selectable Input Gain
- Input/Output for External Noise Reduction System/Equalizer
- 4 Independent Speaker Controls for Fader and Balance
- Independent Mute Function
- Volume Control in 1.25 dB/step
- Low Distortion
- Low Noise and DC Stepping
- Controlled by I^2C Bus Micro-Processor Interface
- Pin-to-Pin Compatible with TDA7313 (for 28-pin version)

Applications

- Car Stereo (Audio)
- Hi-Fi Audio System
- LCD Monitor

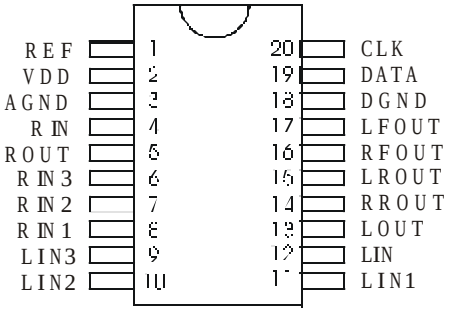
Note: Purchase of I^2C Component of Princeton Technology Corporation (PTC) conveys a license under Philips I^2C Patent Right to use these components in any I^2C System, provided that the system conforms to the I^2C Standard Specification defined by Philips

Block Diagram

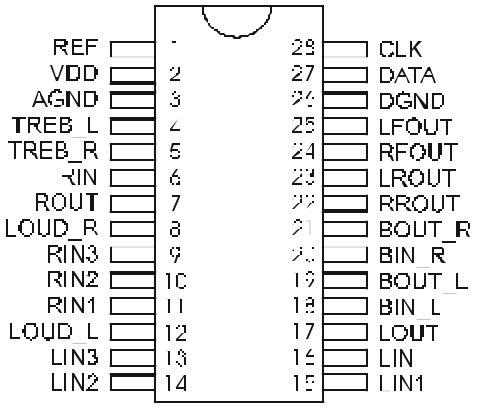


Note: PT2313L (20-pin version) does not provide LOUDNESS Function (LOUD_L/LOUD_R) and Tone Control (TREB_L/TREB_R, BIN_L/BIN_R, BOUT_L/BOUT_R).

Pin Configurations



PT2313L-20



PT2313L

Pin Description

Pin Name	I/O	Description	Pin No.
			28 pins
REF	-	Analog Reference Voltage (1/2VDD)	1
VDD	-	Supply Input Voltage	2
AGND	-	Analog Ground	3
TREB_L	I	Left Channel Input for Treble Controller	4
TREB_R	I	Right Channel Input for Treble Controller	5
RIN	I	Audio processor Right Channel Input	6
ROUT	O	Gain Output and Input Selector for Right Channel	7
LOUD_R	I	Right Channel Loudness Input	8
RIN3	I	Right Channel Input 3	9
RIN2	I	Right Channel Input 2	10
RIN1	I	Right Channel Input 1	11
LOUD_L	I	Left Channel Loudness Input	12
LIN3	I	Left Channel Input 3	13
LIN2	I	Left Channel Input 2	14
LIN1	I	Left Channel Input 1	15
LIN	I	Audio Processor Left Channel Input	16
LOUT	O	Gain Output and Input Selector for Left Channel	17
BIN_L	I	Left Channel Input for Bass Controller	18
BOUT_L	O	Left Channel Output for Bass Controller	19
BIN_R	I	Right Channel Input for Bass Controller	20
BOUT_R	O	Right Channel Output for Bass Controller	21
RROUT	O	Right Rear Speaker Output	22
LROUT	O	Left Rear Speaker Output	23
RFOUT	O	Right Front Speaker Output	24
LFOUT	O	Left Front Speaker Output	25
DGND	-	Digital Ground	26
DATA	I	Control Data Input	27
CLK	I	Clock Input for Serial Data Transmission	28

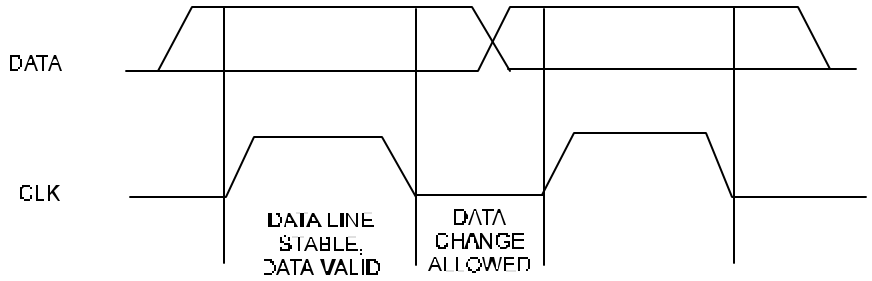
I²C Bus Interface Functional Description

Bus Interface

Data are transmitted to and from the microprocessor to the PT2313L via the DATA and CLK. The DATA and CLK make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

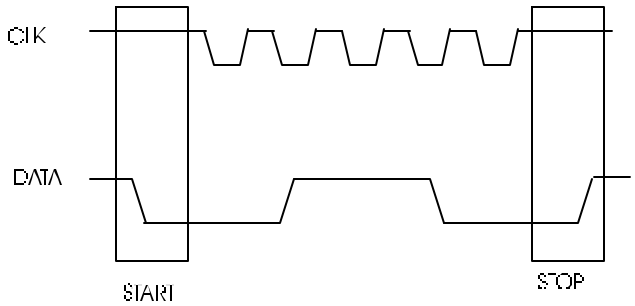
Data Validity

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW States of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



Start and Stop Conditions

A Start Condition is activated when 1) the CLK is set to HIGH and 2) DATA shifts from HIGH to LOW State. The Stop Condition is activated when 1) CLK is set to HIGH and 2) DATA shifts from LOW to HIGH State. Please refer to the timing diagram below.

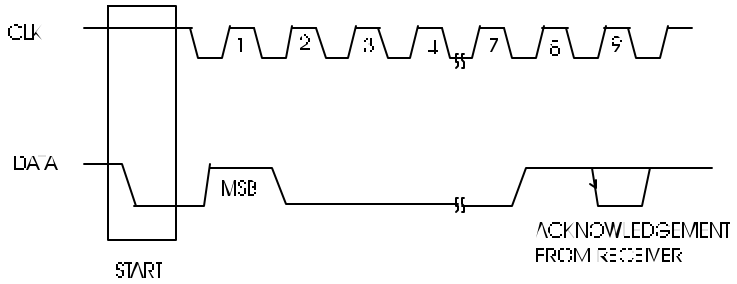


Byte Format

Every byte transmitted to the DATA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

Acknowledge

During the Acknowledge Clock Pulse, the master (µP) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

Transmission without Acknowledge

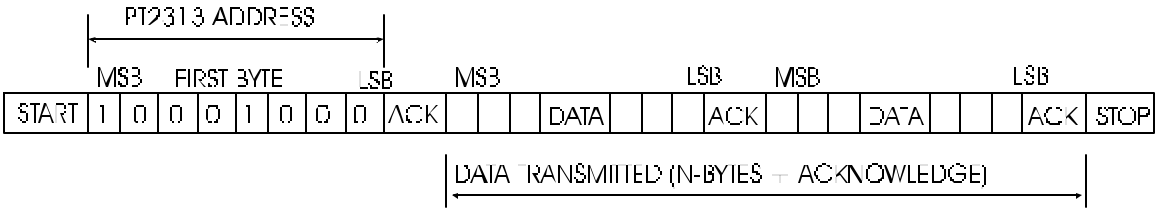
If you want to avoid the acknowledge detection of the audio processor, a simpler µP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

Interface Protocol

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte=88H
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Note: ACK = ACKNOWLEDGE
MAX. CLOCK SPEED = 100KBITS/S

Software Specification

PT2313L Address

PT2313L Address is shown below.

1 **MSB**	**0**	**0**	**0**	**1**	**0**	**0**	**0** **LSB**

Data Bytes

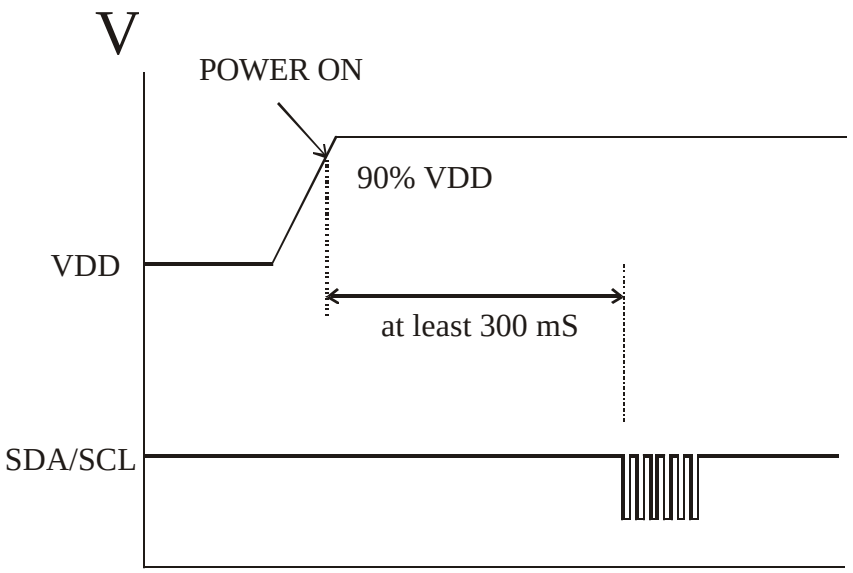
MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bass Control *
0	1	1	1	C3	C2	C1	C0	Treble Control *

where: Ax = 1.25 dB steps; Bx = 10 dB steps; Cx = 2 dB steps; Gx = 3.75 dB/steps

Note: * = Only the 28-pin version provides the Loudness and the Tone Control Functions

I²C Bus Interface Start Time

After Power is turned ON, PT2313L needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. As the Cref value is 10μf, the waiting time period for PT2313L to send I²C Bus Signal is at least 300 ms. If the waiting time period is less than 300 ms, I²C Control may fail. Please refer to the diagram below.



Volume

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25 dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

Speaker Attenuators

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker lF (Right Front) is given by: 1 0 0 1 1 0 0 0.

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25

					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

Audio Switch Data Byte

The following table shows the detailed description of the Audio Switch Data Bytes. For example, (in a 28-pin PT2313l version) a Stereo 1 Input with Gain of +11.25 dB Loudness ON is given by: 0 1 0 0 0 0 0 0.

MSB							LSB	FUNCTION
0	1	0	G1	G0	S2	S1	S0	Audio Switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Stereo 4 *
					0			Loudness ON **
					1			Loudness OFF **
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

Notes: 1. * = Stereo 4 is internally connected.
2. ** = Only available in the 28-pin version.

Bass and Treble Data Bytes *

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by : 0 1 1 1 0 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB

Note: * = This is only applicable for the PT2313L 28-pin version.
The 20-pin version does not provide the Tone Control Function (Treble and Bass).

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Vs	Operating Supply Voltage	10.5	V
Tamb	Operating Ambient Temperature	-40 to +85	^{o}C
Tstg	Storage Temperature Range	-40 to +125	^{o}C

Quick Reference Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Supply Voltage	6	9	10	V
V_{CL}	Max. Input Signal Handling	2	2.5		Vrms
THD	Total Harmonic Distortion (V = 1Vrms, f = 1KHz)		0.07	0.15	%
S/N	Signal to Noise Ratio		95		dB
Sc	Channel Separation (f = 1KHz)		85		dB
	Volume Control 1.25dB step	-75		0	dB
	Bass & Treble Control 2dB step	-14		+14	dB
	Fader & Balance Control 1.25dB step	-37.5		0	dB
GIN	Input Gain 3.75 dB step	0		11.25	dB
AMUTE	Mute Attenuation		85		dB

Electrical Characteristics

(Unless specified: Tamb = 25°C, Vc=9V, RL=100KΩ, Rg = 600Ω, all controls flat (G=0), f=1KHz)

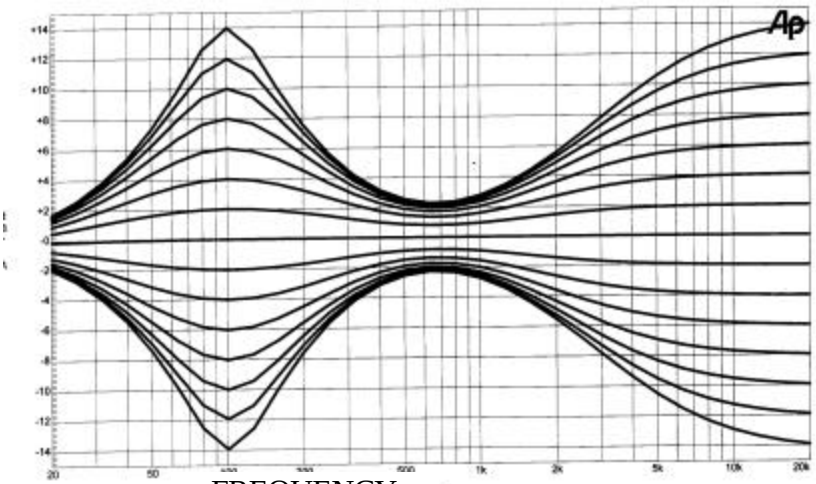
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Supply Voltage		6	9	10	V
Is	Supply Current			30	40	mA
Input Selectors						
R_{II}	Input Resistance	Input 1,2,3	35	50	70	KO
V_{CL}	Clipping Level	Av=-8.75 dB ; d=0.3%	2	2.5		Vrms
S_{IN}	Input Separation (2)		80	100		dB
G_{INmin}	Min. Input Gain		-1	0	1	dB
G_{INmax}	Max. Input Gain			11.25		dB
Volume Control						
C_{RANGE}	Control Range		65	70	75	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		65	70	75	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	AV=0 to -20dB AV=-20 to –60dB	-1.25 -3.0	0	1.25 2	dB dB

Speaker Attenuators	

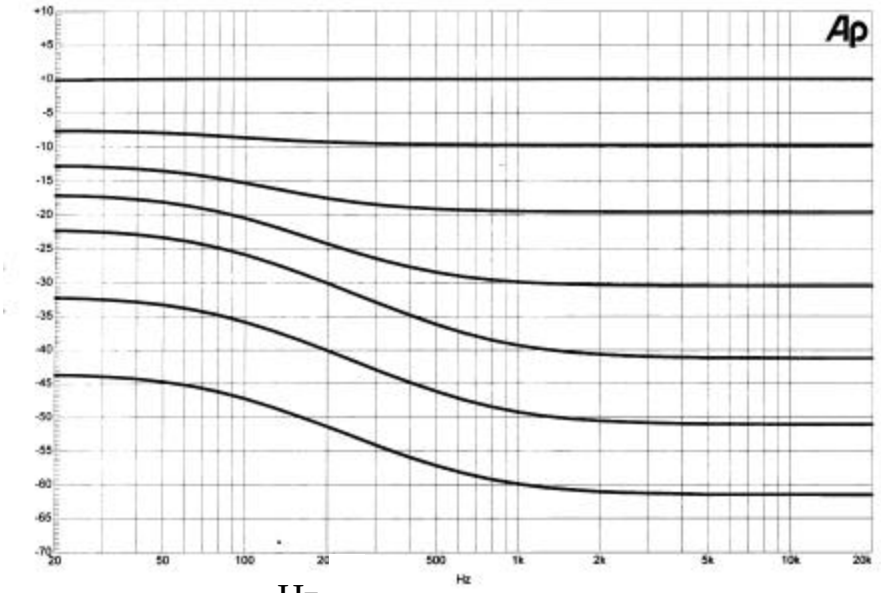
C_{RANGE}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error				1.5	dB
A_{MUTE}	Output Mute Attenuation		70	75		dB
Bass Control (1)						
Gb	Control Range	Max. Boost/Cut	± 12	± 14	± 16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		34	44	58	KO
Treble Control (1)						
Gt	Control Range	Max. Boost/Cut	± 13	± 14	± 15	dB
T_{STEP} Audio Outputs	Step Resolution		1	2	3	dB
V_{OCL}	Clipping Level	AV=-8.75dB, d=0.3%	2	2.5		Vrms
R_{OUT}	Output Resistance		-	40	45	O
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
General						
N_O	Output Noise	BW==20-20KHz, Flat Output Mute All gains=0dB		-97 -92		dB dB
		A Curve All Gains=0dB		-100		dB
S/N	Signal to Noise Ratio	All Gains=0dB Vo=1Vrms		95		dB
d	Distortion	AV=0, VIN=1Vrms AV=-8.75dB, IN=1Vrms AV=-8.75dB, VIN=0.3Vrms		0.1 0.07 0.03	0.3 0.15 0.1	% % %
Sc	Channel Separation Left/Right		80	90		dB
Bus Inputs						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µ A
Vo	Output Voltage SDA Acknowledge	Io=1.6mA			0.4	V

Note: (1) For the Bass and Treble Response, please, refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.

(2) The selected input is grounded thru the 2.2uF capacitor.

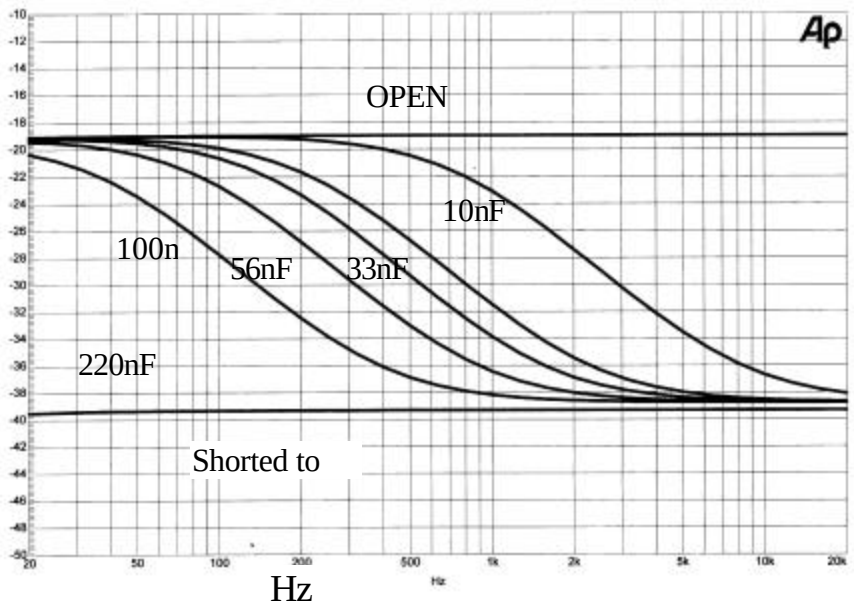


Typical Tone Response (with the ext. Components indicated in the test circuit)



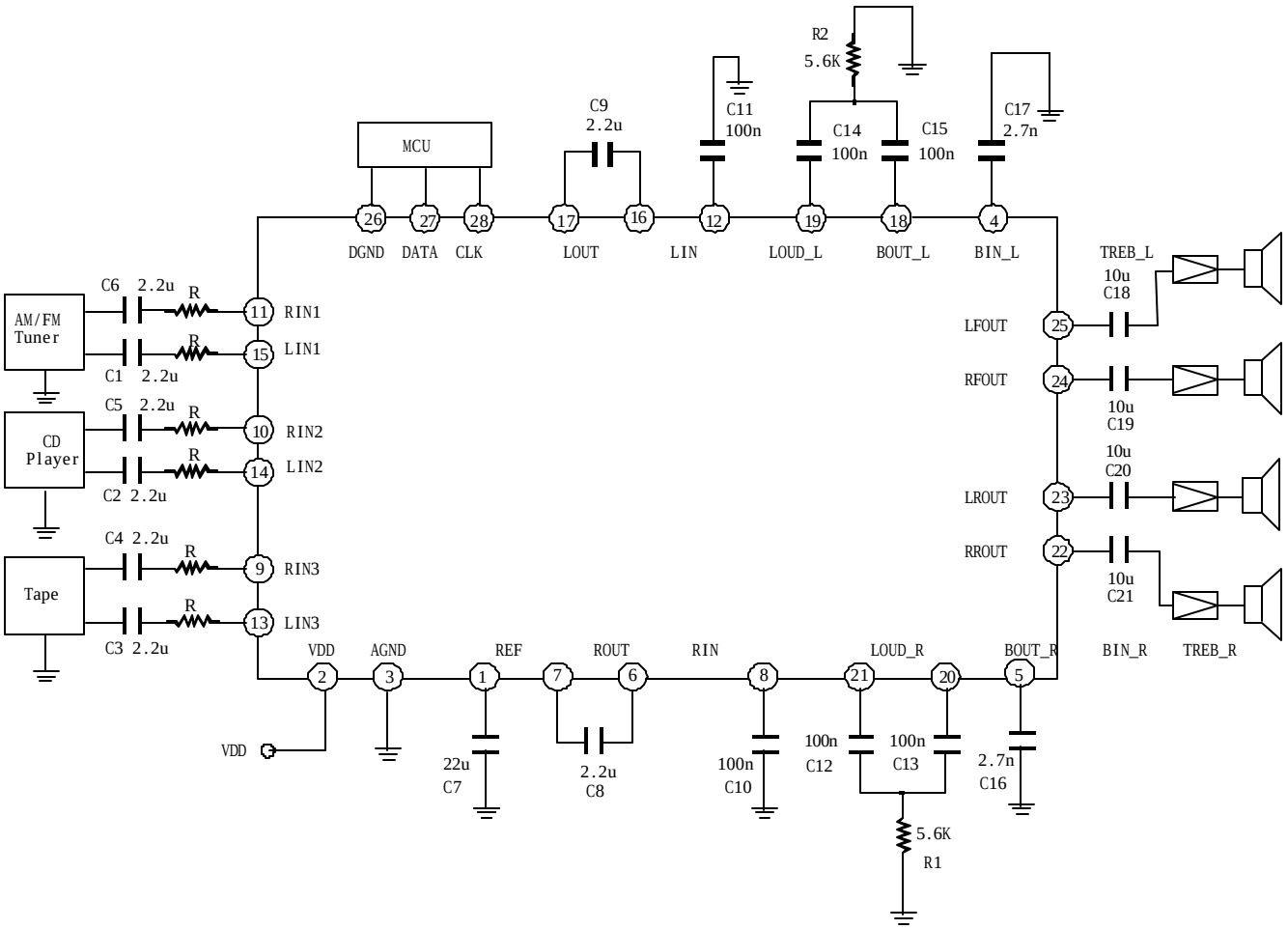
PT2313L: Loudness vs Volume Attenuation Frequency Response (C_{10}=C_{11}=100nF)

dB



PT2313L : C_{10}, C_{11} vs Loudness Frequency Response (Volume=-40dB, All other controls are flat)

Application Circuit



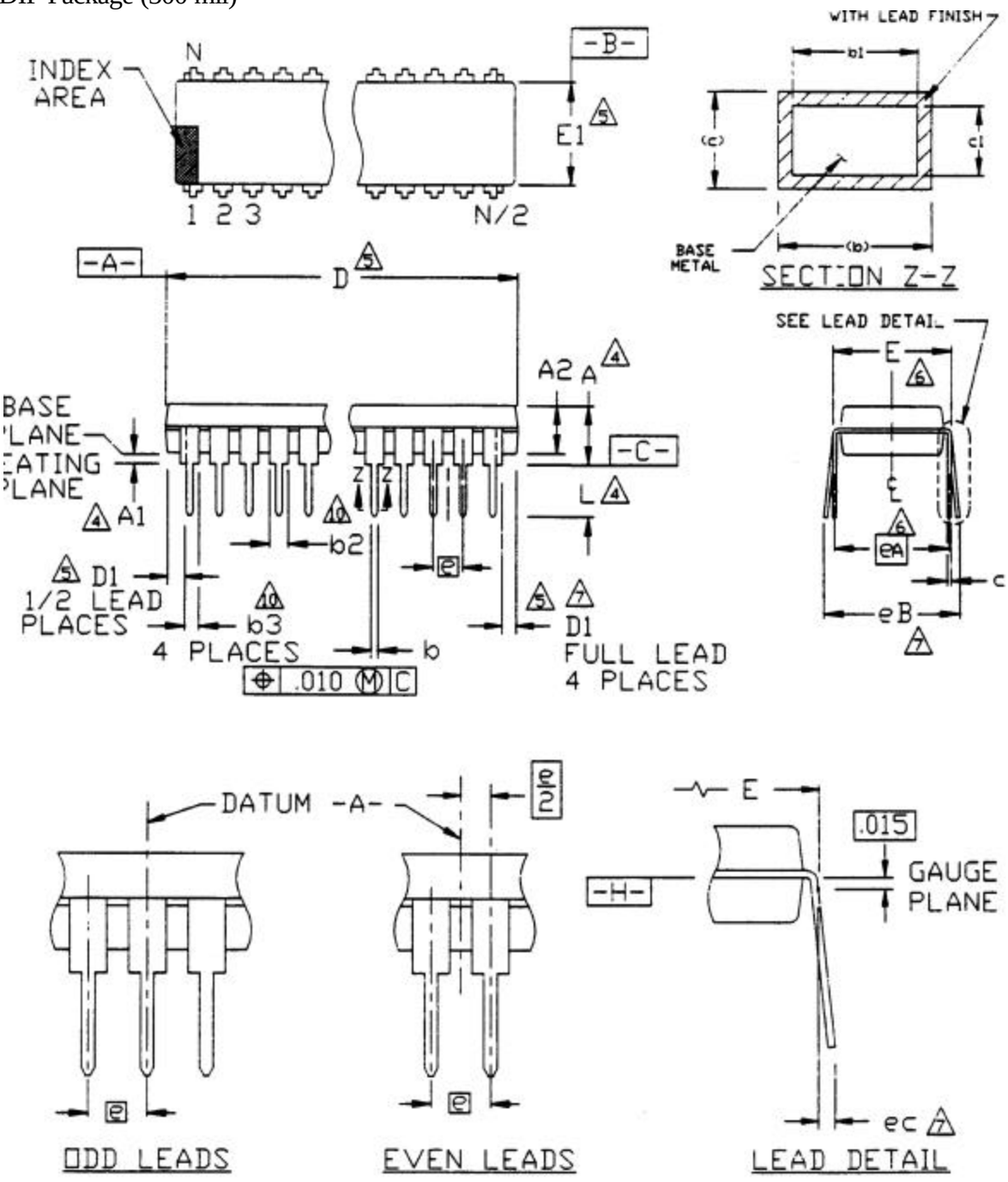
Notes: 1. The Resistor (R) Range = 2.0K Ohms to 3.6 K Ohms.
2. Resistor (R) Recommended Value = 2.4 K Ohms

Order Information

Valid Part Number	Package Type
PT2313L-D	28 Pins, DIP (300 mil)
PT2313L	28 Pins, SOP (300 mil)
PT2313L-20	20 Pins, SSOP (150 mil)

Package Information

28 Pins, DIP Package (300 mil)

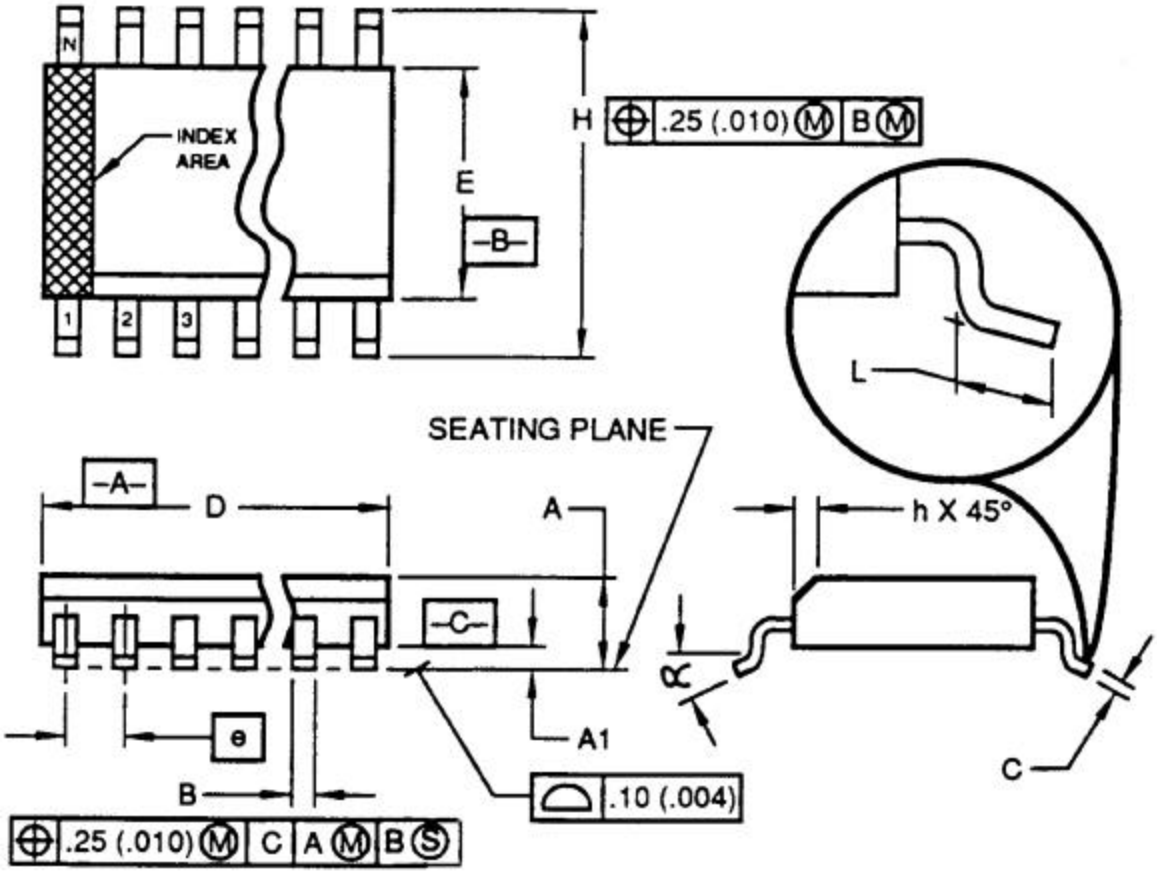


Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	1.345	1.365	1.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	-	0.100 BSC	-
eA	-	0.300 BSC	-
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and eA measured with the leads constrained to be perpendicular to datum -C- .
6. eB and eC are measured at the lead tips with the leads constrained.
7. N is the number of terminal positions (N=28)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010" (0.25mm).
10. This variation is a ½ lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- incident with the bottom of lead where lead exits body.
13. Refer to JEDEC MS-001 Variation BF.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

28 Pins, SO Package (300 mil)

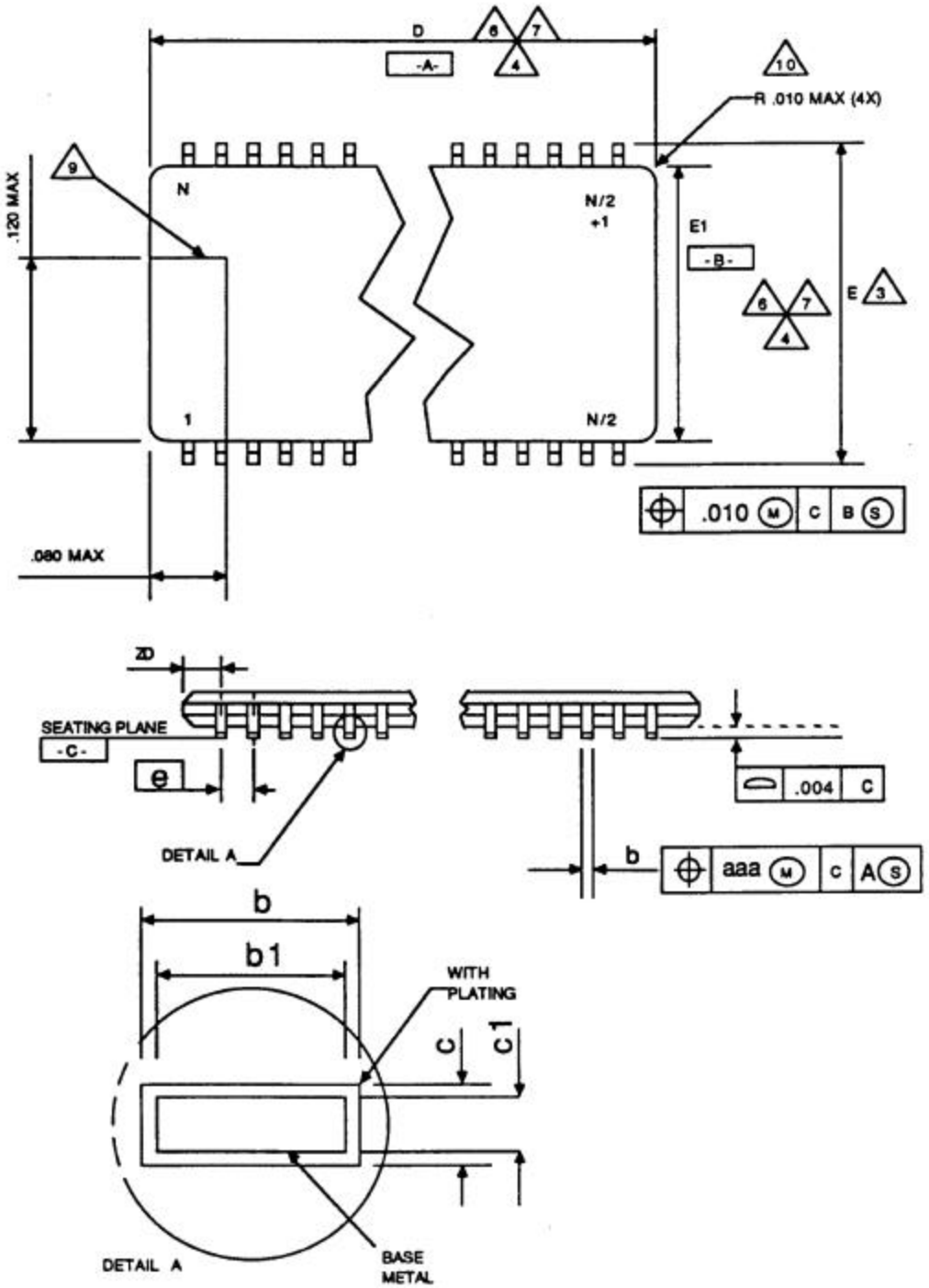


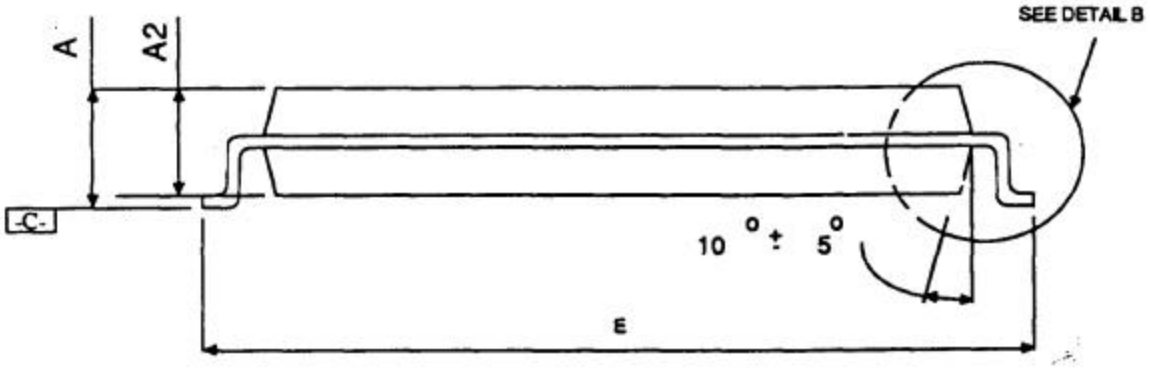
Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 bsc	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0^o	8^o

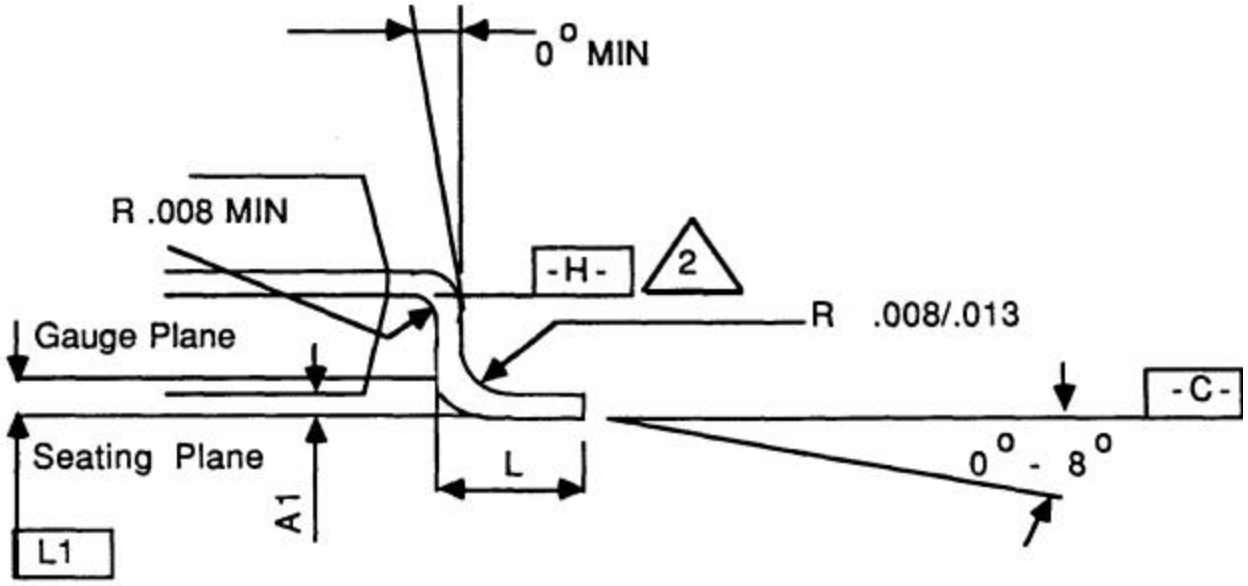
Notes: 1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash and protrusion shall not exceed 0.15mm (0.016in) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of terminal for soldering to a substrate.
6. N is the number of terminal positions (N=28).
7. The lead width B as measured 0.36mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024 in).
8. Controlling dimension: MILLIMETER
9. Refer to JEDEC MS-013 Variation AE.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

20 Pins, SSOP Package (150 mil)




A
A2
SEE DETAIL B
-C-
10° ± 5°
E


0° MIN
R .008 MIN
-H-
2
R .008/.013
Gauge Plane
-C-
Seating Plane
L
0° - 8°
A1
L1

DETAIL B

Symbol	Min.	Nom.	Max
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.059
b	0.008	-	0.012
b1	0.008	0.010	0.011
c	0.007	-	0.010
c1	0.007	0.008	0.009
D	0.337	0.341	0.344
ZD	0.058 REF		
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
L	0.016	0.025	0.050
L1	0.010 BASIC		
e	0.025 BASIC		
aaa		0.007	

Notes:
1. Dimensioning and tolerancing conform to ANSI Y14.5M-1982.
2. Datum Plane -H- pincident with bottom of lead, where lead exits body.
3. To be determined at seating plane -C-
4. Datums -A- and -B- to be determined at datum .
5. Controlling Dimension: Inches
6. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.006" per side. Dimension E1 does not include interlead mold protrusions. Interlead mold protrusions shall not exceed "0.010" per side.
7. To be determined at plane -H- .
8. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.002" at least material condition.
9. Details of pin1 identifier are optional but must be located within the zone indicated.
10. N is the number of leads (N=20)
11. Dimension ZD is for reference only. Minimum ZD dimension shall be 0.001" more than half of b dimension such that no exposed leadframe material is allowed for end leads.
12. Refer to JEDEC MO-137 variation AD.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION